# NCS2003, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

# High Slew Rate, Low Voltage, Rail-to-Rail Output Operational Amplifiers

The NCS2003 family of op amps features high slew rate, low voltage operation with rail−to−rail output drive capability. The 1.8 V operation allows high performance operation in low voltage, low power applications. The fast slew rate and wide unity−gain bandwidth (5 MHz at 1.8 V) make these op amps suited for high speed applications. The low input offset voltage (4 mV max) allows the op amp to be used for current shunt monitoring. Additional features include no output phase reversal with overdriven inputs and ultra low input bias current of 1 pA.

The NCS2003 family is the ideal solution for a wide range of applications and products. The single channel NCS2003, dual channel NCS20032, and quad channel NCS20034 are available in a variety of compact and space−saving packages. The NCV prefix denotes that the device is AEC−Q100 Qualified and PPAP Capable.

### Features

- Unity Gain Bandwidth: 7 MHz at $V_S$ = 5 V
- Fast Slew Rate: 8 V/μs rising, 12.5 V/μs falling at $V_S$ = 5 V
- Rail−to−Rail Output
- No Output Phase Reversal for Over−Driven Input Signals
- Low Offset Voltage: 0.5 mV typical
- Low Input Bias Current: 1 pA typical
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Current Shunt Monitor
- Signal Conditioning
- Active Filter
- Sensor Buffer

### End Products

- Motor Control Drives
- Hard Drives
- Medical Devices
- White Goods and Air Conditioners

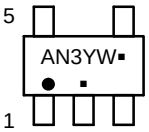
This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

**ON Semiconductor®**

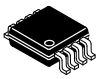
www.onsemi.com

**MARKING DIAGRAMS**

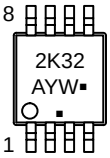

**SOT23−5**
**CASE 483**
**(NCS/NCV2003)**




**SOT553, 5 LEAD**
**CASE 463B**
**(NCS2003)**

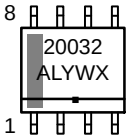



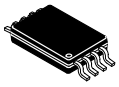
**Micro8™**
**DM SUFFIX**
**CASE 846A**



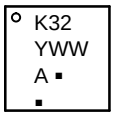


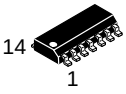
**SOIC−8**
**CASE 751**



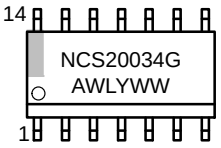



**TSSOP−8**
**T SUFFIX**
**CASE 948S**




**SOIC−14 NB**
**CASE 751A**



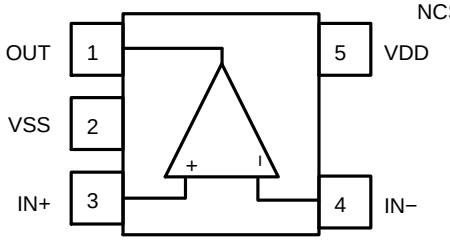

A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

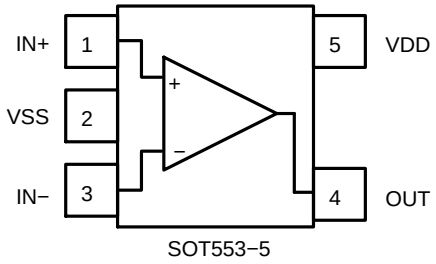
(Note: Microdot may be in either location)

### ORDERING INFORMATION

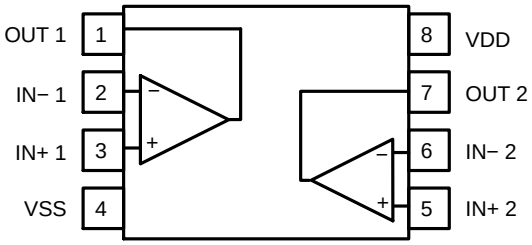
See detailed ordering and shipping information on page 2 of this data sheet.

**Single Channel Configuration**
NCS2003, NCV2003




**Dual Channel Configuration**
NCS20032, NCV20032




**Quadruple Channel Configuration**
NCS20034, NCV20034

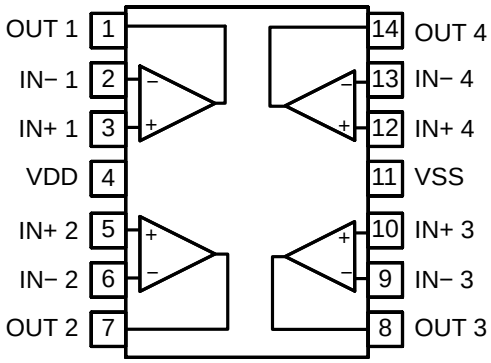



**Figure 1. Pin Connections**

## ORDERING INFORMATION

| Device | Configuration | Automotive | Marking | Package | Shipping† |
|---|---|---|---|---|---|
| NCS2003SN2T1G | Single | No | AN3 | SOT23−5 (Pb−Free) | 3000 / Tape and Reel |
| NCS2003XV53T2G | | | A3 | SOT553−5 (Pb−Free) | 4000 /Tape and Reel |
| NCV2003SN2T1G* | | Yes | AN3 | SOT23−5 (Pb−Free) | 3000 / Tape and Reel |
| NCS20032DMR2G (In Development)** | Dual | No | 2K32 | Micro8 (Pb−Free) | 4000 / Tape and Reel |
| NCS20032DR2G (In Development)** | | | 20032 | SOIC−8 (Pb−Free) | 2500 / Tape and Reel |
| NCS20032DTBR2G (In Development)** | | | K32 | TSSOP−8 (Pb−Free) | 3000 / Tape and Reel |
| NCV20032DMR2G* (In Development)** | | Yes | 2K32 | Micro8 (Pb−Free) | 4000 / Tape and Reel |
| NCV20032DR2G* (In Development)** | | | 20032 | SOIC−8 (Pb−Free) | 2500 / Tape and Reel |
| NCV20032DTBR2G* (In Development)** | | | K32 | TSSOP−8 (Pb−Free) | 3000 / Tape and Reel |
| NCS20034DR2G | Quad | No | NCS20034G | SOIC−14 (Pb−Free) | 2500 / Tape and Reel |
| NCV20034DR2G* | | Yes | NCS20034G | SOIC−14 (Pb−Free) | 2500 / Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
**Contact local sales office for more information.

## ABSOLUTE MAXIMUM RATINGS

Over operating free−air temperature, unless otherwise stated

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$ − $V_{SS}$) | | $V_S$ | 7.0 | V |
| **INPUT AND OUTPUT PINS** | | | | |
| Input Voltage (Note 1) | | $V_{IN}$ | $V_{SS}$ − 0.3 to 7.0 | V |
| Input Current | | $I_{IN}$ | 10 | mA |
| Output Short Current (Note 2) | | $I_O$ | 100 | mA |
| **TEMPERATURE** | | | | |
| Storage Temperature | | $T_{STG}$ | −65 to 150 | °C |
| Junction Temperature | | $T_J$ | 150 | °C |
| **ESD RATINGS** (Note 3) | | | | |
| Human Body Model | NCx2003<br>NCx20034 | HBM | 3000<br>3000 | V |
| Machine Model | NCx2003<br>NCx20034 | MM | 200<br>150 | V |
| Charged Device Model | NCx2003<br>NCx20034 | CDM | 1000<br>2000 | V |
| **OTHER PARAMETERS** | | | | |
| Moisture Sensitivity Level (Note 5) | | MSL | Level 1 | |
| Latch−up Current (Note 4) | | $I_{LU}$ | 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Neither input should exceed the range of $V_{SS}$ − 300 mV to 7.0 V. This device contains internal protection diodes between the input pins and $V_{DD}$. When $V_{IN}$ exceeds $V_{DD}$, the input current should be limited to the specified value.
2. Indefinite duration; however, maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 and JESD22−A114
   ESD Machine Model tested per AEC−Q100−003 and JESD22−A115
   ESD Charged Device Model tested per AEC−Q100−011 and ANSI/ESD S5.3.1−2009
4. Latch−up current tested per JEDEC Standard JESD78.
5. Moisture Sensitivity Level tested per IPC/JEDEC standard J−STD−020A.

## THERMAL INFORMATION

| Thermal Metric | Symbol | Package | Value | Unit |
|---|---|---|---|---|
| Junction to Ambient Thermal Resistance | $\theta_{JA}$ | SOT23−5/TSOP−5 | 235 | °C/W |
| | | SOT553−5 | 250 | |
| | | Micro8/MSOP8 | 238 | |
| | | SOIC−8 | 190 | |
| | | TSSOP−8 | 140 | |
| | | SOIC−14 | 156 | |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Operating Supply Voltage ($V_{DD}$ − $V_{SS}$) | | $V_S$ | 1.7 | 5.5 | V |
| Specified Operating Range | NCS2003<br>NCV2003, NCx20032, Ncx20034 | $T_A$ | −40<br>−40 | +85<br>+125 | °C |
| Input Common Mode Range | | $V_{CM}$ | $V_{SS}$ | $V_{DD}$−0.6 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS: $V_S$ = +1.8 V

At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to midsupply, $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | | 0.5 | 4.0 | mV |
| | | | | | | **5.0** | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | | **2.0** | | μV/°C |
| Input Bias Current | $I_{IB}$ | | | | 1 | | pA |
| Input Offset Current | $I_{OS}$ | | | | 1 | | pA |
| Channel Separation | XTLK | DC, NCx20032, NCx20034 | | | 100 | | dB |
| Input Resistance | $R_{IN}$ | | | | >1 | | TΩ |
| Input Capacitance | $C_{IN}$ | | | | 1.2 | | pF |
| Common Mode Rejection Ratio | CMRR | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ – 0.6 V | | 70 | 80 | | dB |
| | | $V_{IN}$ = $V_{SS}$ + 0.2 V to $V_{DD}$ – 0.6 V | | **65** | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | $R_L$ = 10 kΩ | | 80 | 92 | | dB |
| | | | | **75** | | | |
| | | $R_L$ = 2 kΩ | | | 92 | | |
| | | | | **70** | | | |
| Output Current Capability (Note 6) | $I_{SC}$ | Sourcing | | 5 | 8 | | mA |
| | | Sinking | | 10 | 14 | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 10 kΩ | | **1.75** | 1.798 | | V |
| | | $R_L$ = 2 kΩ | | **1.7** | 1.78 | | |
| Output Voltage Low | VOL | $R_L$ = 10 kΩ | NCx2003 | | 7 | **50** | mV |
| | | | NCx20034 | | 7 | **100** | |
| | | $R_L$ = 2 kΩ | | | 20 | **100** | |
| **NOISE PERFORMANCE** | | | | | | | |
| Voltage Noise Density | $e_N$ | f = 1 kHz | | | 20 | | nV/√Hz |
| Current Noise Density | $i_N$ | f = 1 kHz | | | 0.1 | | pA√Hz |
| **DYNAMIC PERORMANCE** | | | | | | | |
| Gain Bandwidth Product | GBWP | | | | 5 | | MHz |
| Slew Rate at Unity Gain | SR | Rising Edge, $R_L$ = 2 kΩ, $A_V$ = +1 | | | 6 | | V/μs |
| | | Falling Edge, $R_L$ = 2 kΩ, $A_V$ = +1 | | | 9 | | |
| Phase Margin | $\psi_m$ | $R_L$ = 10 kΩ, $C_L$ = 5 pF | | | 53 | | ° |
| Gain Margin | $A_m$ | $R_L$ = 10 kΩ, $C_L$ = 5 pF | NCx2003 | | 12 | | dB |
| | | | NCx2003x | | 8 | | |
| Settling Time | $t_S$ | $V_O$ = 1 Vpp, Gain = 1, $C_L$ = 20 pF | Settling time to 0.1% | | 1.8 | | μs |
| Total Harmonics Distortion + Noise | THD+N | $V_O$ = 1 $V_{pp}$, $R_L$ = 2 kΩ, $A_V$ = +1, f = 1 kHz | | | 0.015 | | % |
| | | $V_O$ = 1 $V_{pp}$, $R_L$ = 2 kΩ, $A_V$ = +1, f = 10 kHz | NCx2003 | | 0.025 | | |
| | | | NCx2003x | | 0.003 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by design and/or characterization.

### ELECTRICAL CHARACTERISTICS: $V_S$ = +1.8 V

At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to midsupply, $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| Power Supply Rejection Ratio | PSRR | NCx2003 | | 72 | 80 | | dB |
| | | | | **65** | | | |
| | | NCx20032, NCx20034 | | **80** | 100 | | |
| Quiescent Current | $I_{DD}$ | No load, per channel | NCx2003 | | 230 | 560 | μA |
| | | | | | | **1000** | |
| | | | NCx20032, NCx20034 | | 275 | 375 | |
| | | | | | | **575** | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by design and/or characterization.

### ELECTRICAL CHARACTERISTICS: $V_S$ = +5.0 V

At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to midsupply, $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | 0.5 | 4.0 | mV |
| | | | | | **5.0** | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | **2.0** | | μV/°C |
| Input Bias Current | $I_{IB}$ | | | 1 | | pA |
| Input Offset Current | $I_{OS}$ | | | 1 | | pA |
| Channel Separation | XTLK | DC, NCx20032, NCx20034 | | 100 | | dB |
| Input Resistance | $R_{IN}$ | | | >1 | | TΩ |
| Input Capacitance | $C_{IN}$ | | | 1.2 | | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design and/or characterization.

## ELECTRICAL CHARACTERISTICS: $V_S$ = +5.0 V

At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to midsupply, $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Common Mode Rejection Ratio | CMRR | NCx2003 | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ – 0.6 V | 65 | 90 | | dB |
| | | | $V_{IN}$ = $V_{SS}$ + 0.2 V to $V_{DD}$ – 0.6 V | **63** | | | |
| | | NCx20032, NCx20034 | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ – 0.6 V | 70 | 90 | | |
| | | | $V_{IN}$ = $V_{SS}$ + 0.2 V to $V_{DD}$ – 0.6 V | **65** | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | $R_L$ = 10 kΩ | | 86 | 92 | | dB |
| | | | | **78** | | | |
| | | $R_L$ = 2 kΩ | | 83 | 92 | | |
| | | | | **78** | | | |
| Output Current Capability (Note 7) | $I_{SC}$ | Sourcing | | 40 | 76 | | mA |
| | | Sinking | | 50 | 96 | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 10 kΩ | | **4.95** | 4.99 | | V |
| | | $R_L$ = 2 kΩ | | **4.9** | 4.97 | | |
| Output Voltage Low | VOL | $R_L$ = 10 kΩ | NCx2003 | | 8 | **50** | mV |
| | | | NCx20034 | | 8 | **100** | |
| | | $R_L$ = 2 kΩ | | | 24 | **100** | |
| **NOISE PERFORMANCE** | | | | | | | |
| Voltage Noise Density | $e_N$ | f = 1 kHz | | | 20 | | nV/√Hz |
| Current Noise Density | $i_N$ | f = 1 kHz | | | 0.1 | | pA√Hz |
| **DYNAMIC PERORMANCE** | | | | | | | |
| Gain Bandwidth Product | GBWP | | | | 7 | | MHz |
| Slew Rate at Unity Gain | SR | Rising Edge, $R_L$ = 2 kΩ, Av = +1 | | | 8 | | V/μs |
| | | Falling Edge, $R_L$ = 2 kΩ, Av = +1 | | | 12.5 | | |
| Phase Margin | $\psi_m$ | $R_L$ = 10 kΩ, $C_L$ = 5 pF | NCx2003 | | 64 | | ° |
| | | | Ncx20034 | | 56 | | |
| Gain Margin | $A_m$ | $R_L$ = 10 kΩ, $C_L$ = 5 pF | | | 9 | | dB |
| Settling Time | $t_S$ | $V_O$ = 1 $V_{pp}$, Gain = 1, $C_L$ = 20 pF | Settling time to 0.1% | | 0.6 | | μs |
| Total Harmonics Distortion + Noise | THD+N | $V_O$ = 4 $V_{pp}$, $R_L$ = 2 kΩ, $A_V$ = +1, f = 1 kHz | NCx2003 | | 0.005 | | % |
| | | | NCx2003x | | 0.001 | | |
| | | $V_O$ = 4 $V_{pp}$, $R_L$ = 2 kΩ, $A_V$ = +1, f = 10 kHz | | | 0.01 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design and/or characterization.

**ELECTRICAL CHARACTERISTICS: $V_S$ = +5.0 V**

At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to midsupply, $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| Power Supply Rejection Ratio | PSRR | NCx2003 | | 72 | 80 | | dB |
| | | | | **65** | | | |
| | | NCx20032, NCx20034 | | **80** | 100 | | |
| Quiescent Current | $I_{DD}$ | No load, per channel | NCx2003 | | 300 | 660 | μA |
| | | | | | | **1000** | |
| | | | NCx20032, NCx20034 | | 325 | 450 | |
| | | | | | | **675** | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design and/or characterization.

## TYPICAL CHARACTERISTICS

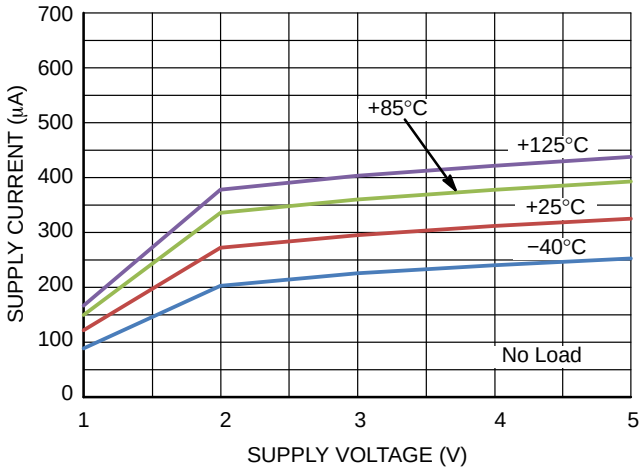



**Figure 2. Quiescent Supply Current vs. Supply Voltage**

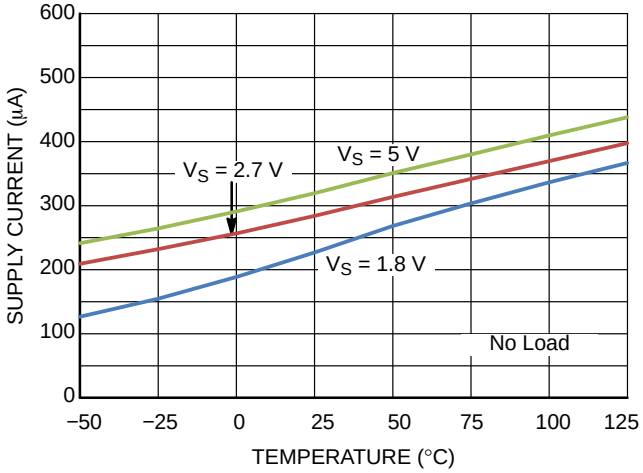



**Figure 3. Quiescent Supply Current vs. Temperature**

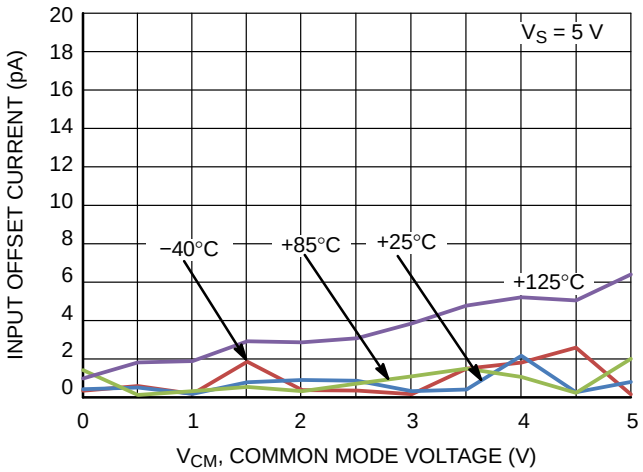



**Figure 4. Input Offset Current vs. $V_{CM}$**

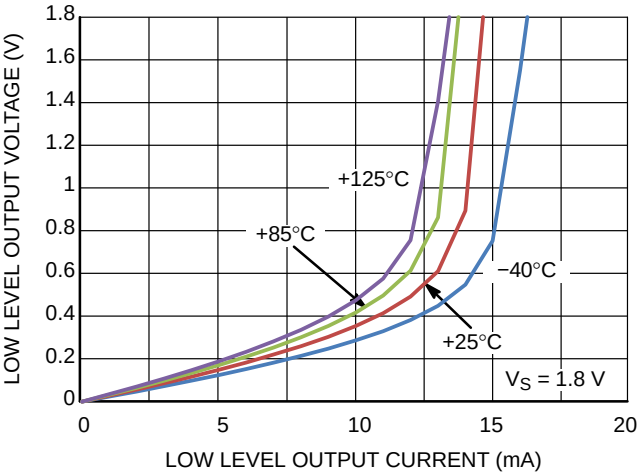



**Figure 5. Low Level Output Voltage vs. Output Current @ $V_S$ = 1.8 V**

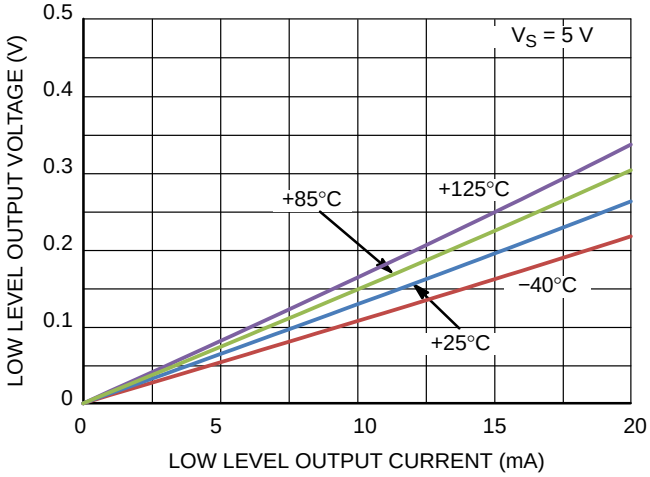



**Figure 6. Low Level Output Voltage vs. Output Current @ $V_S$ = 5 V**

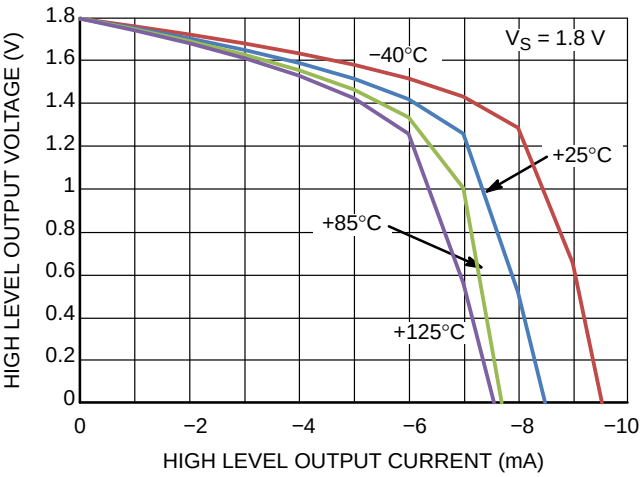



**Figure 7. High Level Output Voltage vs. Output Current @ $V_S$ = 1.8 V**

## TYPICAL CHARACTERISTICS

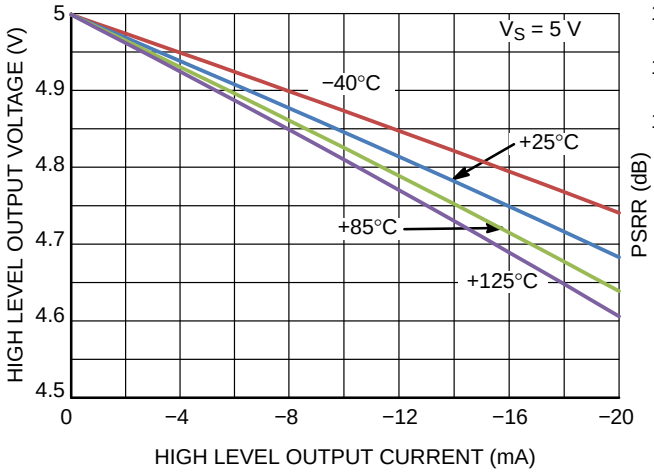



**Figure 8. High Level Output Voltage vs. Output Current @ $V_S$ = 5 V**

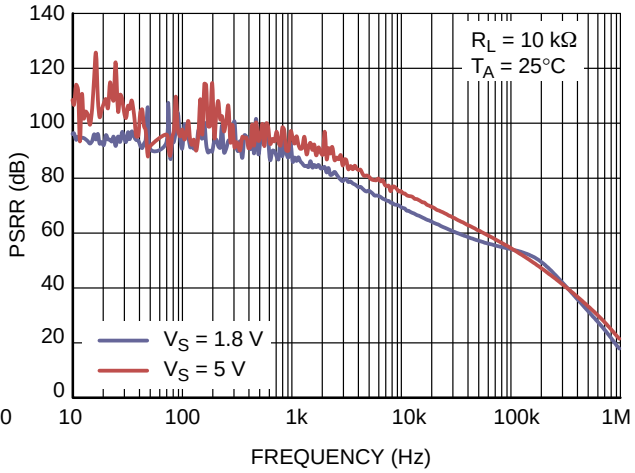



**Figure 9. PSRR vs. Frequency**

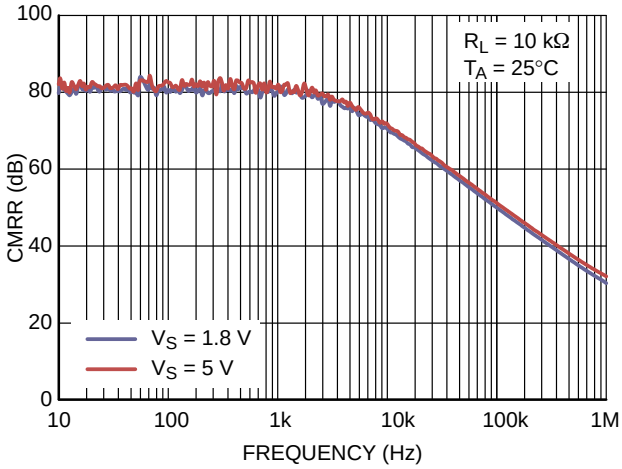



**Figure 10. CMRR vs. Frequency**

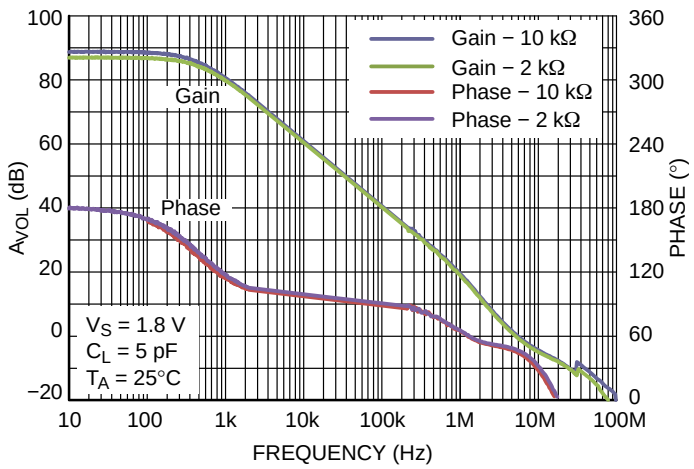



**Figure 11. Open Loop Gain and Phase vs. Frequency @ $V_S$ = 1.8 V**

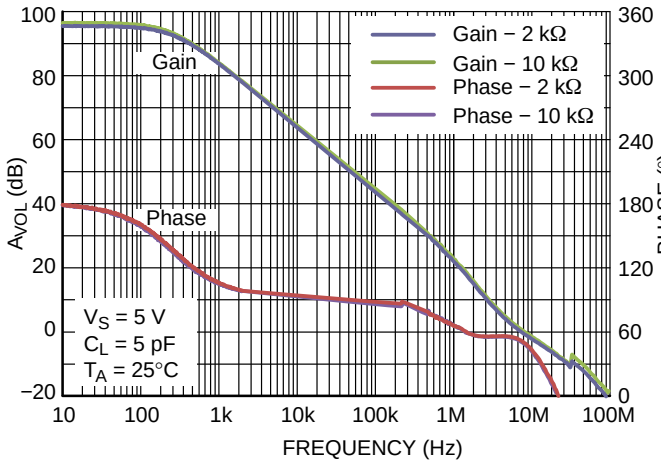



**Figure 12. Open Loop Gain and Phase vs. Frequency @ $V_S$ = 5 V**

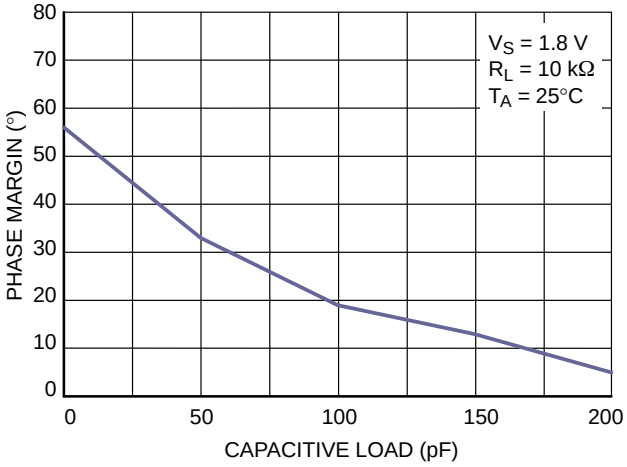



**Figure 13. Phase Margin vs. Capacitive Load**

## TYPICAL CHARACTERISTICS

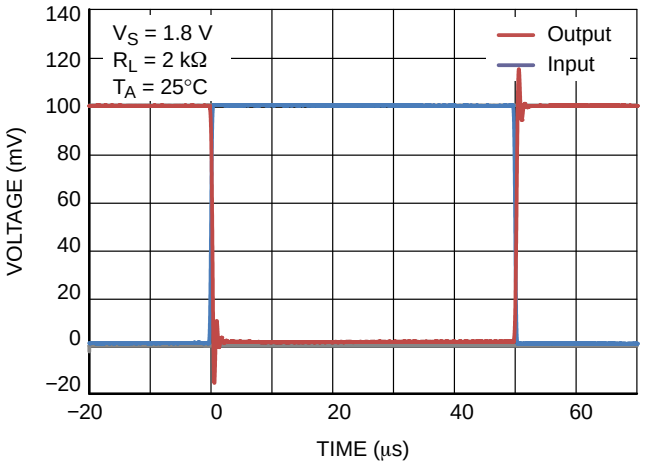



**Figure 14. Inverting Small Signal Transient Response**

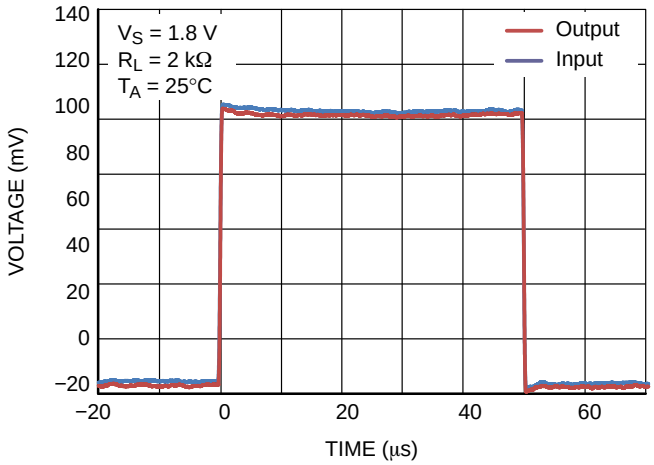



**Figure 15. Non−Inverting Small Signal Transient Response**

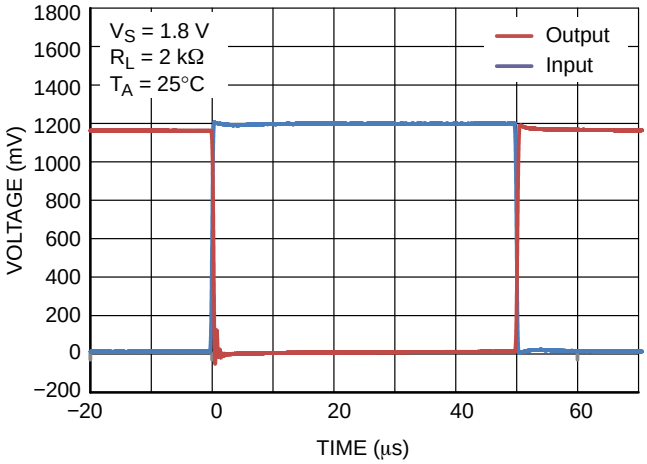



**Figure 16. Inverting Large Signal Transient Response**

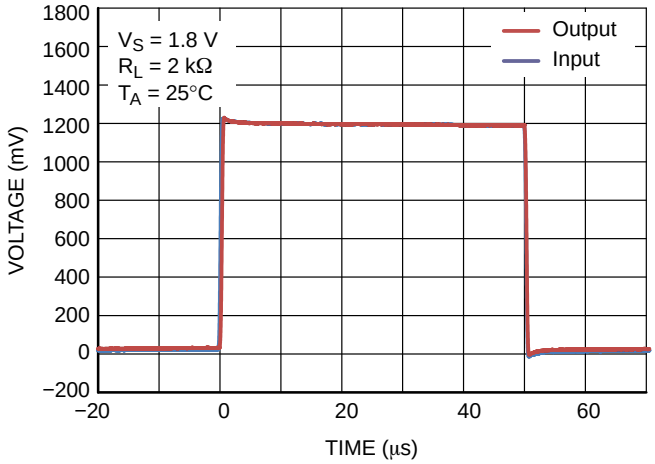



**Figure 17. Non−Inverting Large Signal Transient Response**

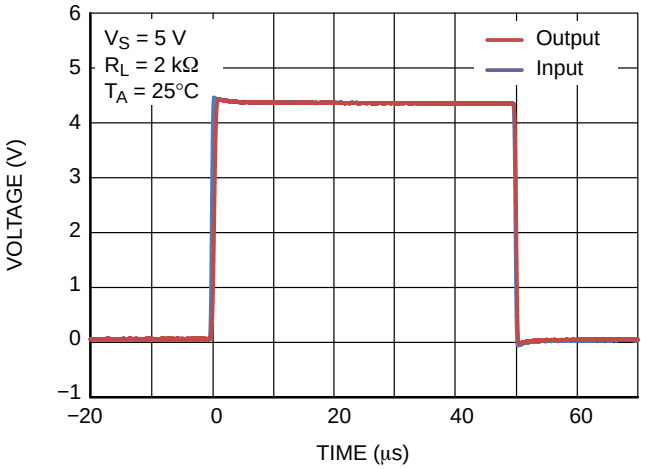



**Figure 18. Non−Inverting Large Signal Transient Response**

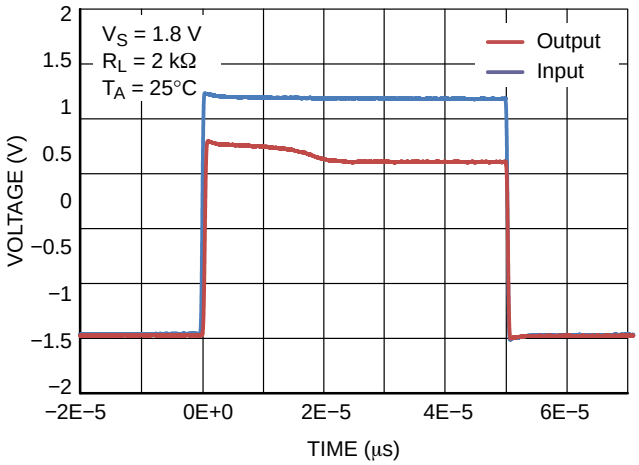



**Figure 19. Output Overload Recovery**

## TYPICAL CHARACTERISTICS

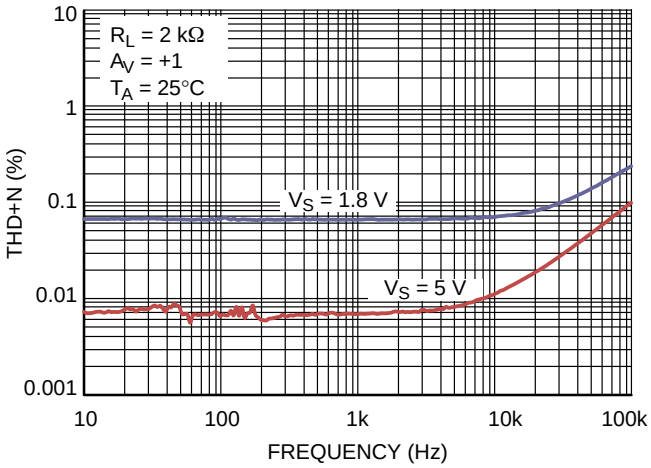



**Figure 20. THD+N vs. Frequency**

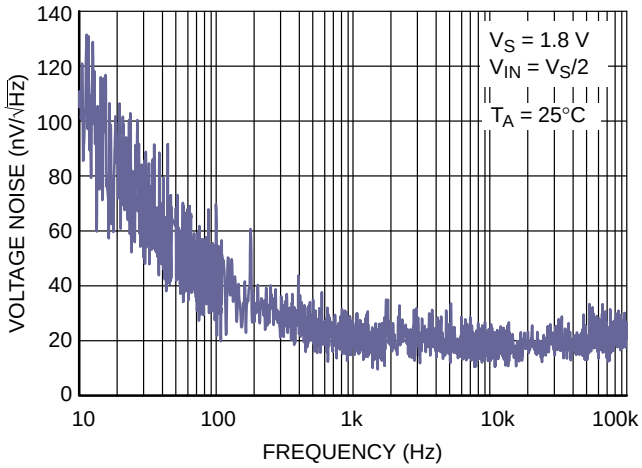



**Figure 21. Input Voltage Noise vs. Frequency**

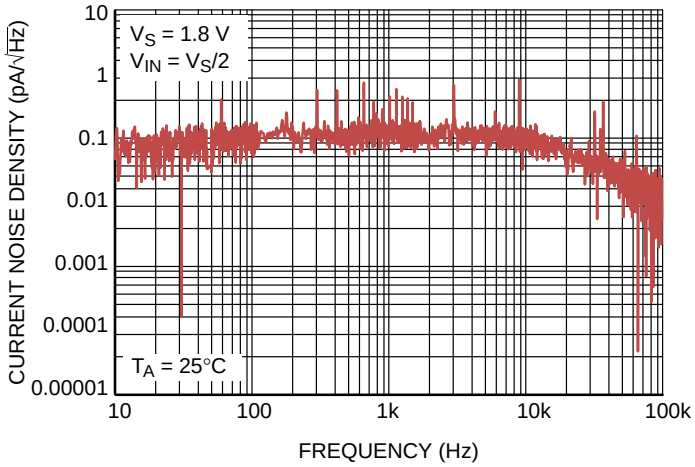
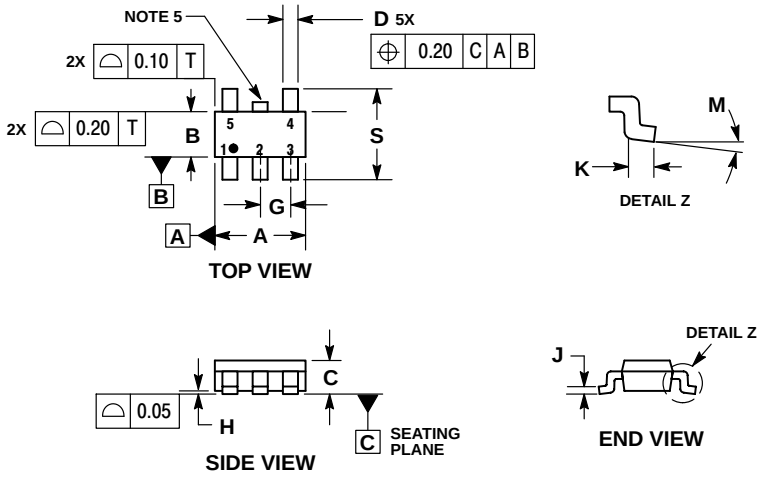



**Figure 22. Noise Density vs. Frequency**

## PACKAGE DIMENSIONS

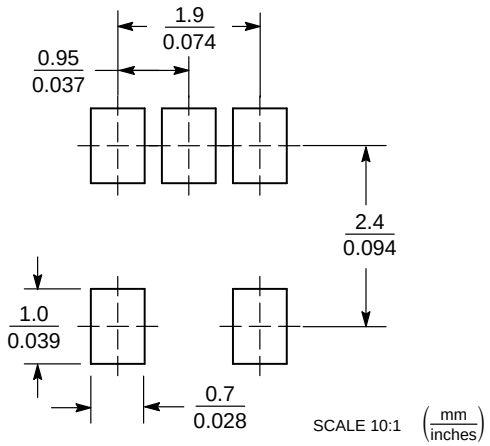
**TSOP−5**
CASE 483−02
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 3.00 BSC | |
| B | 1.50 BSC | |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| M | 0 ° | 10 ° |
| S | 2.50 | 3.00 |

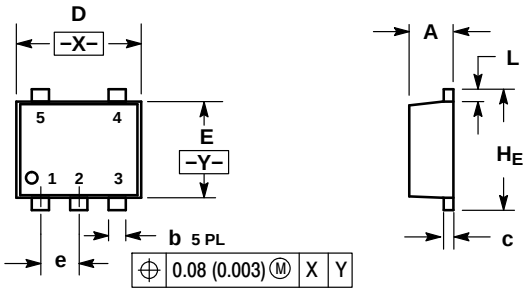
## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

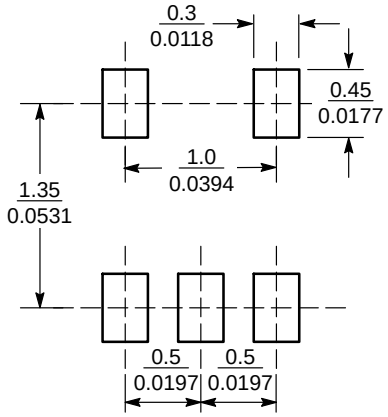
**SOT−553, 5 LEAD**
CASE 463B
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.08 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |
| E | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| e | | 0.50 BSC | | | 0.020 BSC | |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| $H_E$ | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |

**RECOMMENDED SOLDERING FOOTPRINT***

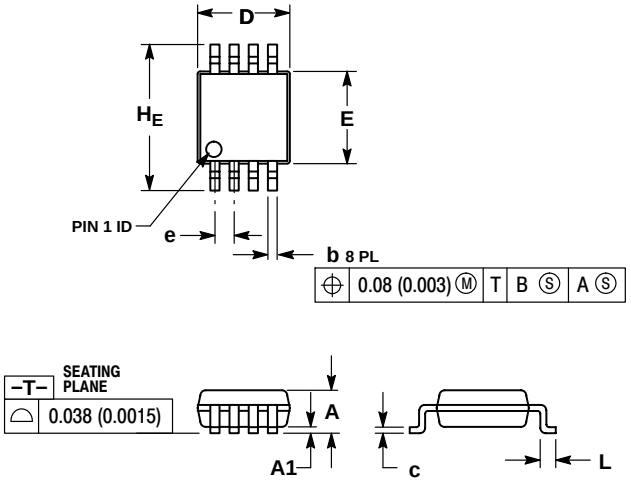



SCALE 20:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

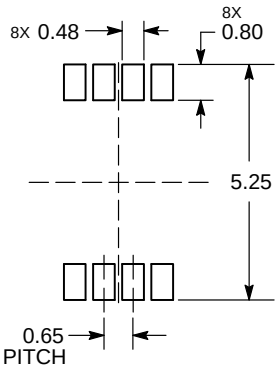
**Micro8™**
CASE 846A−02
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | −− | −− | 1.10 | −− | −− | 0.043 |
| A1 | 0.05 | 0.08 | 0.15 | 0.002 | 0.003 | 0.006 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.013 | 0.016 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.021 | 0.028 |
| $H_E$ | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |

## RECOMMENDED SOLDERING FOOTPRINT*

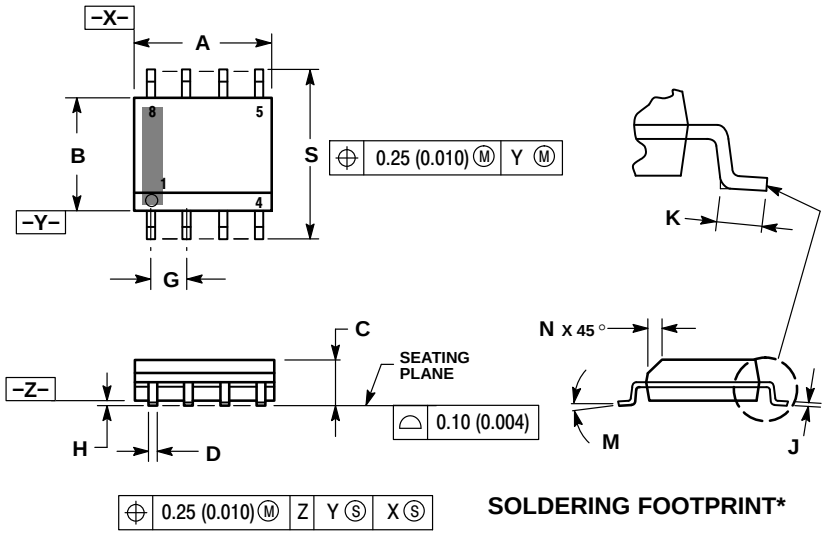



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

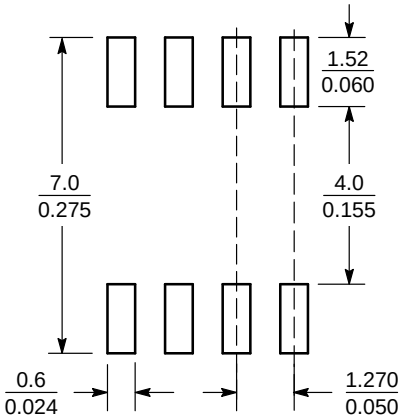
**SOIC−8 NB**
CASE 751−07
ISSUE AK




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

**SOLDERING FOOTPRINT***

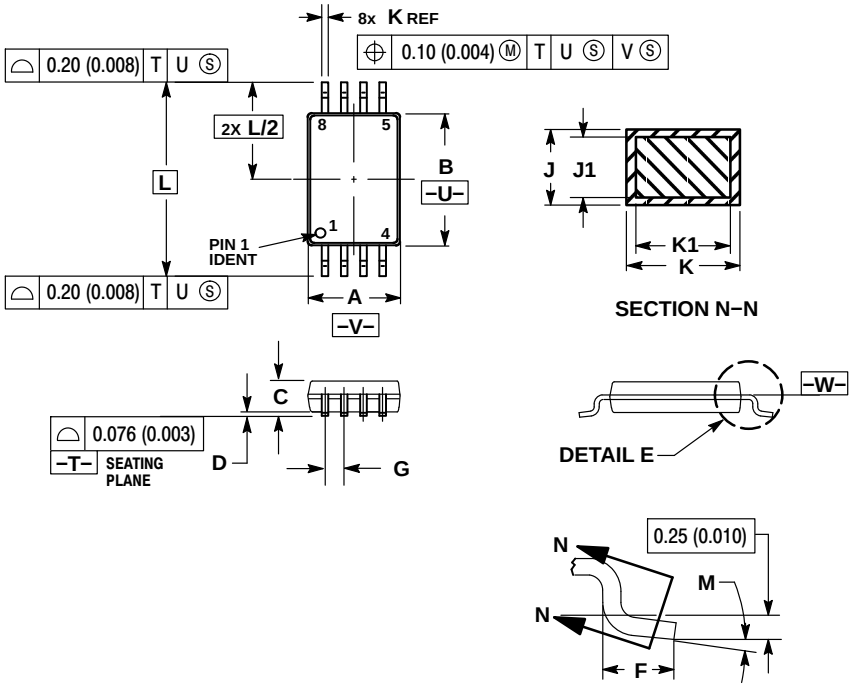



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**TSSOP−8**
CASE 948S
ISSUE C

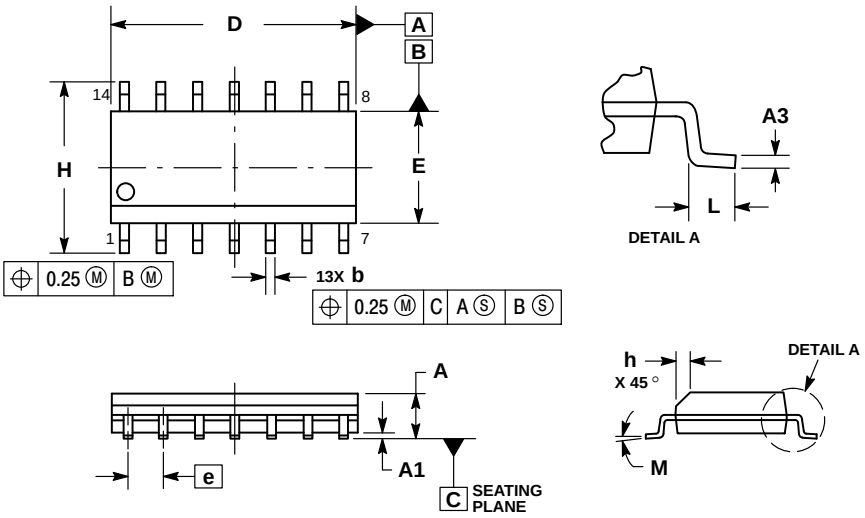



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

## PACKAGE DIMENSIONS

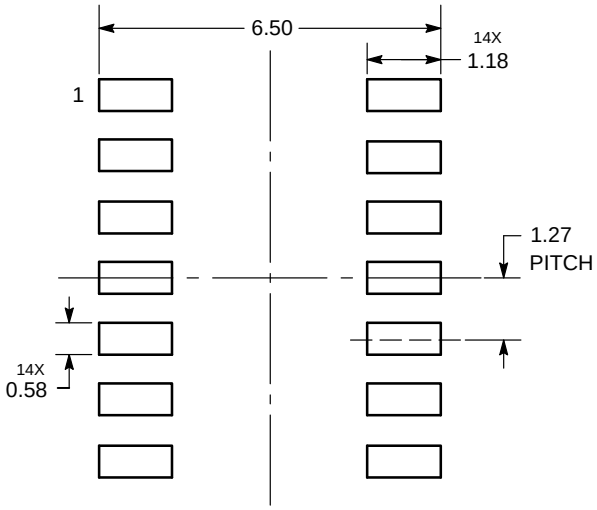
**SOIC−14 NB**
CASE 751A−03
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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